

The Image Processor based on Signal Ranking, Determination of Rank Differences with their subsequent Selection and Weighted Addition

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Abstract— In order to expand the functionality by increasing the number and complexity of nonlinear multi-input functions and transformations performed, in this paper we consider the urgent need for creating high-performance hardware image processors (IP). Such IPs are designed based on a conceptual approach, the essence of which is to rank the processed signals (pixels), fast command-controlled selection of rank differences with their subsequent weight addition. And since these procedures are basic for all advanced models of convolutional neural networks (CNNs), such IP can play the role of not only high-speed pre-filtering devices, but also be self-learning reconfigurable accelerators for CNNs, associative memory models, clustering and pattern recognition. First, we briefly review related works in order to show the advantages of using the proposed concept and equivalence models (EMs). The capacity and recognition properties of NNs based on modified EMs exceed the similar indicators of traditional networks by orders of magnitude. Therefore, such EM-neuroparadigm is promising for processing, recognition of large-sized images, including highly correlated, high-noise images. And since the main nodes of EMs are filtering nodes and procedures with continuous-logical operations, in this article we consider approaches to the design of IPs with extended functionality. The proposed structure of the processor based on our concept and the FPGA Altera EP3C16F484 Cyclone III family chip. The design results and calculations show that it is possible to implement IP for an image size of 64*64 and a window of 3*3 in a single crystal. For 2.5 V and a clock frequency of 200MHz, the power consumption will be at the level of 200mW, and the time for calculating the filter pixels will be 25ns. The results confirm the correctness of the concept.

Keywords—image processor, signal ranking, selection, weighted addition; equivalental model, rank differences, neuron-equivalentor, convolutional neural network.

I. INTRODUCTION, OVERVIEW, ANALYSIS OF PUBLICATIONS AND FORMULATION OF WORK GOAL

Advanced direction becomes fast parallel images processing using optoelectronics for interconnects and non-conventional MIMO-system, corresponding matrix logics (ML) (continuous, neural-fuzzy and others) and corresponding mathematical apparatus [1-5]. Photodetectors can be monolithically integrated with digital electronics in silicon, which allows the realization of stacked 3-D chip architecture in principle and significantly simplifies design of OE-VLSI circuits [2]. Smart image sensors with ADC [4, 5] show a great application field and potential. Our approach favors smart pixel architecture combining parallel signal detection with parallel processing in circuit, what guarantees the fastest processing. For self-learning neural networks (NN) based on equivalency models (EM) [6, 7], the elements of MLs are required. For the description and modeling of each continual subject domain and the class of its tasks, its own logical-algebraic apparatus (LAA) is required. Formal LAA is based on clear rules that allow you to make an exact description of a certain class of problems and even suggest an algorithm for solving them. The basis of information technologies in the analog field is precisely the continual LAAs: infinite-valued logic [8], continuous logic with all its variants and generalizations, additive-multiplicative logic (AM) algebra, predicate selection algebra, equivalence algebra [6-7]. They determined the biologically inspired stage of development of LAAs and new more energy-efficient direction of models and hardware implementations of artificial intelligence. Many logics are based on multi-input operations *min* (x_1, x_2, \dots, x_n) and *max* (x_1, x_2, \dots, x_n). The image processing algorithms, basic procedures of composition-decomposition, fuzzy inference in artificial neural-fuzzy systems are also based on multi-input min-max operations. Therefore, is an urgent need

to improve the nodes, that perform these and similar operations. Efficiency increasing of systems of speed images processing in the use of special mathematical support. The special place among such methods occupies the class of the nonlinear algorithms that carried out transformation of kind: $\mathbf{B}=\{b_{k,l}\}=\mathbf{F}(\mathbf{A})=\{\Phi_{k,l}(\mathbf{A}_{k,l})\}$, where $\Phi_{k,l}(\mathbf{A}_{k,l})$ — nonlinear function, which is determined by subset of rank and (or) index statistician of selection. By virtue of the last this subclass was adopted by rank algorithms.

The algorithms of extreme filtration, using values of *min* and *max* on samples of neighborhood space, are the special cases of the rank algorithms. Any r -th index statisticians $v_s(\mathbf{r})$ of display (k, l) the set neighboring of which form other (N_s-1) the elements of selection it is possible to bind to the local histograms of distributing of values of neighboring elements and with the proper functions of the well-organized choice $F_n^m(\mathbf{X})$ element, where $\mathbf{X} = (x_1, x_2, \dots, x_n)$. Such functions at any values of changing variables choose that size which at the location all right not decreasing are occupied by m -th place. These functions can be represented by a logical formula: $F^{(r)}(x_1, x_2, \dots, x_n) = x^{(r)}$, $r=1 \div n$, where r -rank of the base operations of continuous logic (CL). Thus for $r = n$ this operation passes to n -local disjunction, for $r=1$ to n -local conjunction. The algebra formed in a number of $C = [0, 1]$ with base operations $f(r)$ and complementarity operation $(-)$ is named ordering Boolean algebra. Rank algorithms are locally-adaptive on the same essence: simplicity of local adaptation, invariance to spatial links and to signals dimension, almost algorithms complication independence from the sizes of neighboring. Sorting algorithms have been widely researched due to the need for sorting in many applications. In paper [9] approaches to creation of programmable relational processors for sorting were shown. But in such a relational processor, working with analog signals, the sorting structure for ordering signals is complex.

Therefore, the aim is to simplify and digitize the sorting node to build on its basis the relational processors of nonlinear image processing. The latter can be used as nodes of ordinal logic, data ordering and sorting nodes, rank filters, fragment classifier recognizers, as tools for morphological operations as dilation, erosion, opening, closing. The above mentioned *min-max* operations on sets of signals are also necessary, which represent structural windows or selected fragments processed images. Many of the morphological operations need to be repeated many times and for all the fragments of the image being processed, therefore, there is an urgent need to reduce the execution time of *min-max* operations and ranking operations. Therefore, the **goal of our work** is to search new options for implementing both signal sorting nodes, including digital, providing increased accuracy and speed, and based on them relational non-linear image processing processor with advanced functionality. In addition, taking into account the recent emergence of a new element base, our task is to prove the possibility of creating on the FPGA, practically in one chip, an image preprocessor (IP) with enhanced technical characteristics and a wide range of commands through the use of a new method of processing pre-ranked signals and (or) their differences. To achieve this goal, it is necessary to simulate the algorithms and methods

themselves, and then based on them design and simulate the technical options for the implementation of non-linear IP and their main nodes.

The main computational procedure of most known methods and algorithms used in the creation of biometric systems of machine vision and recognition of objects in images is the comparison of fragments of the current processed image with a template image. The mutual two-dimensional correlation function or convolution with a filter is the most common discriminant measure of mutual matching-comparison of the reference fragment with the current image fragment. At the same time, in the works [10, 11, 12] it was shown that to improve the discriminant properties and quality of recognition-comparison, especially for strongly correlated and noise-damaged images, it is desirable to use recognition methods based on mutual equivalent two-dimensional spatial functions, nonlinear transformations and adaptive-correlation weighting. Therefore, to solve the problems of image recognition and clustering using new spatially invariant models of neural networks, equivalence models (EMs) of autoassociative memory (AAM) and heteroassociative memory (HAM) were proposed [11-15]. Studies of such EMs have shown that these models allow better recognition of images with increased dimensions (vectors with $1024 \div 4096$ components) and a significant percentage (up to 25-30%) of damage, while the capacity of the AAM can be an order of magnitude higher than the number of neurons representing vector arrays, the set of which is memorized [12, 14, 15]. In addition, it is known that for scene analysis and recognition it is necessary to first solve not only the problem of preliminary filtering, but also the problem of object clustering. Such preliminary clustering allows organizing proper automated data grouping, conducting cluster analysis, evaluating each cluster based on many features, assigning a class label, and improving subsequent training and classification procedures. Since significant advantages of EM were demonstrated when creating on their basis advanced multiport AAM and HAM, neural networks (NN) for parallel cluster analysis of images [7, 15, 16], the current task was to study a more general, spatially invariant (SI) equivalence model (SI EM). Namely, such models that are invariant to spatial displacements require a large number of comparisons of image fragments [7, 16, 17]. And comparisons are basic operations in the most promising paradigms of convolutional neural networks (CNN) with deep learning [7, 17]. In our previous article [7], we considered the issues of new possible ways of self-learning in such extended models, explained some important fundamental concepts of various associative recognition and understanding the principles of functioning of biologically inspired NN-structures, simulated processing processes in them [1], trained and extracted patterns in such models, and also proposed their implementation. In article [17], the authors showed that the concept of self-learning works directly with multi-level images. In SI EM, we calculate spatially dependent normalized equivalence functions (SD_NEF), the elements of which will correspond to the value of the normalized equivalence of the fragment of the input image \mathbf{X} and one of the selected fragments from the training matrix. To implement ESLCNS [1, 17], we need some new or modified known devices capable of

calculating normalized spatial equivalence functions (NSEqF) with the required speed and performance. For all known convolutional neural networks, as well as for our equivalence models, it is necessary to calculate the convolution of the current image fragment in each layer with a large number of templates that are used, selected or formed during the training process. However, as studies show, large images require a large number of filters for image processing, and the size of the filters can also be large. Therefore, there is an acute problem of increasing the computational performance of hardware implementations of such convolutional neural networks.

II. PRESENTATION OF THE MAIN RESEARCH RESULTS

A. Design of the main unit of Image Processor

Our proposed allows ranking of signals and forming output signals are shown in Fig. 1. Structure of digital multifunctional image processor (IP) DMIP_2 based on FPGA with serial input and registers memory to form a vector of signals to be sorted and 1 output using sorting unit (SU) based on modified conveyor homogeneous wave structure (MCHWS) consisting of layers of digital comparison switching circuits is shown in Fig.2. Here variant DMIP_1 with 10 inputs and 1 output and supply of all input signals in parallel is not shown. For the convenience of data input, we have developed and modeled a processor DMIP_2 circuit with register memory for fast sequential image input and automatic sequential search of processed windows. It is shown in Fig. 2. Simulation results of DMIP_2 are shown in Fig. 3, 4.

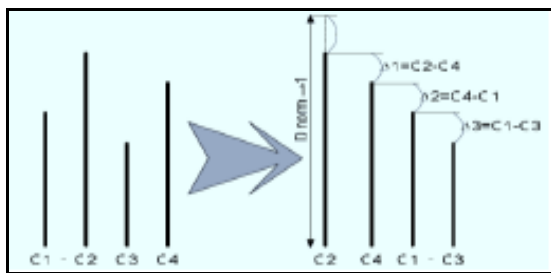


Figure 1. Graphical representation of the processor operations of ranking.

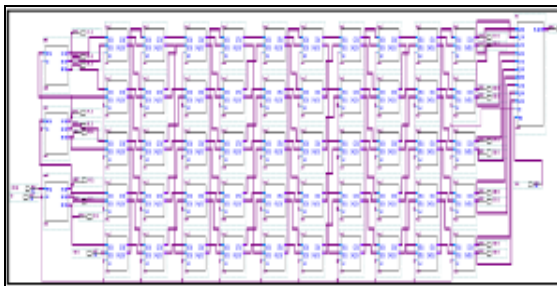


Figure 2. FPGA Structure of DMIP_2 with serial input and registers memory to form a vector of signals to be sorted and 1 output.

Since such processor have output signals that are ranked by value and not by difference of values, by some modification [9, 18, 19, 20] they can be used to organize an additional calculation of the difference of signals having neighboring ranks. Besides, the difference in signal values is also necessary for such a function as nonequivalence. Based on the operations of bounded difference and nonequivalence, a whole set of

other continuous logic complex operations and functions are constructed. For example, early we can select one of n signals by rank using multiplexer. There is only 1 output (ranks). And now we can also form signals difference between max signal and next by order. So we can find signal that is proportional to difference of any two signals from ordered set. Such approach allows to formed output complement signals. If one of reference level is $D=1$ (255) than difference between the reference and any of signals is the complement of the signal. Therefore, we will develop this idea further, taking into account the fact that the selection, amplification, weighting and addition of signals are simple.

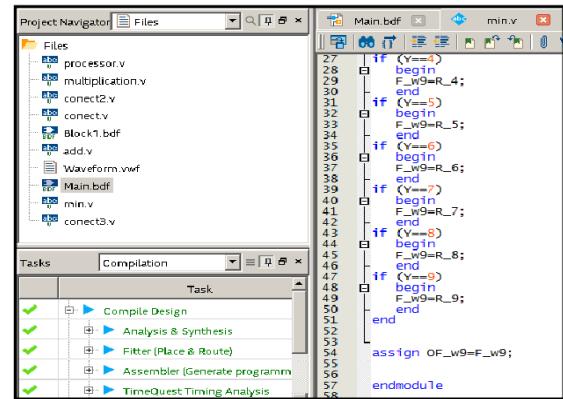


Figure 3. Simulation of DMIP_2 based on FPGA (window fragments).

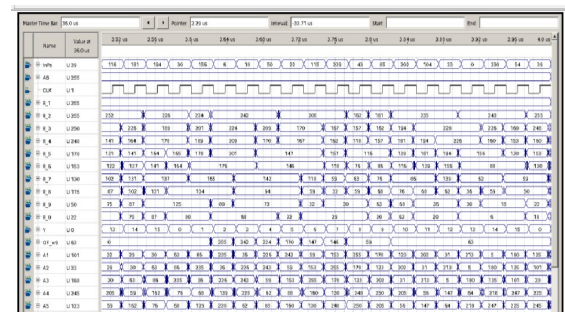


Figure 4. Simulation results of DMIP_2 based on FPGA with serial input and registers memory and 1 output (issuing ranks, one switch)

B. Modeling of digital multifunctional image processor

The simulation results of DMIP_3 (Fig. 5) with serial input and registers memory, 2 outputs for rank and rank differences signals weighing-selection processing are shown in Fig. 6-9. As can be seen from Fig. 3, 4, 6, 7 the resources of the Altera FPGA chip EP3C16F484

Cyclone III family are not fully used in the first case, and in the second for the processor with register memory and two outputs almost completely (there is a small margin).

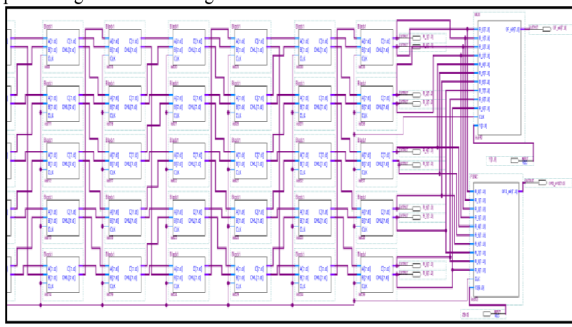


Figure 5. Structure of DMIP_3 based on FPGA with serial input and registers memory to form a vector of signals to be sorted, 2 outputs for rank and rank differences signals weighing-selection processing.

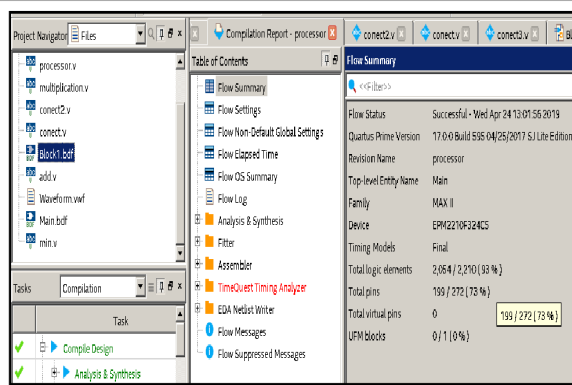


Figure 6. Simulation of DMIP_3 based on FPGA with serial input and 2 output (window fragments).

The processing cycle in the pipelined structure of DMIP and SU did not exceed 25 nanoseconds, which makes it possible to achieve an input / output rate of pixels of the processed and processed images at the level of 40MHz. During the processing cycle, DMIP_1 essentially performs (9*ln9-estimates for the best algorithms!) Sorting operations and generates all the ranks and their differences, which gives, taking into account the wide variety of output functions, performance estimates of at least 10^9 operations per second.

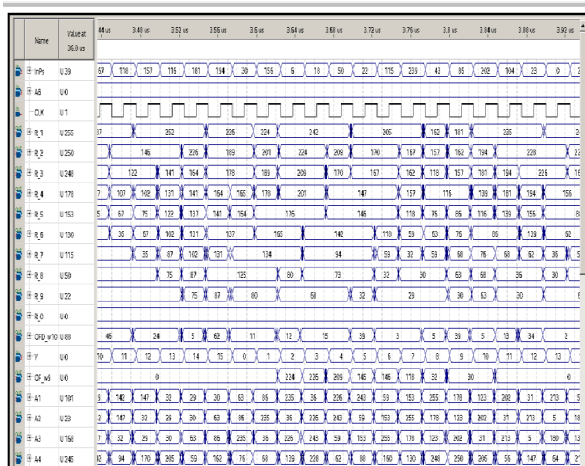


Figure 7. Simulation results of DMIP_3 with 2 outputs (issuing ranks, two switches) in case of formation of a difference of ranks r2-r3.

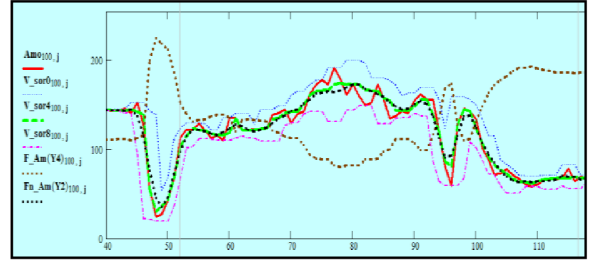


Figure 8. A good example of image line processing using proposed DMIP: Original line (red) and received rank and other output functions.

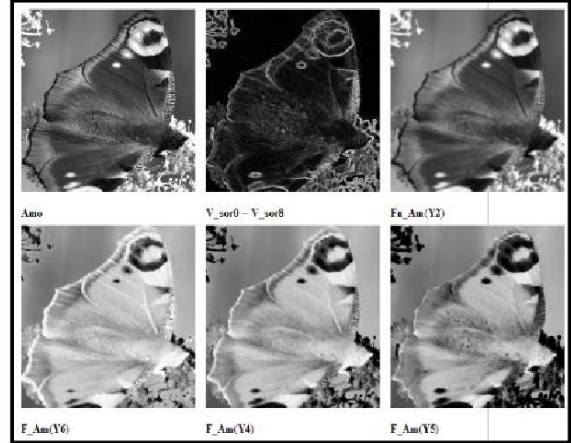


Figure 9. The results of the Amo image transformations using DMIP for different rank values and different functions defined by the control vector Y.

III. DISCUSSION

The results obtained confirm the correctness of the chosen concept and the possibility of creating digital multifunctional image processors with an expanded set of nonlinear signal processing operations, including rank and its modifications. In addition, such processors can be easily and quickly and efficiently configured for the desired type and function of processing-transformation. At the same time, it should be noted that with an increase in the size of the filters, i.e. the number of signals to be ranked, the costs of sorting-ranking when implemented in digital formats and the duration of the operation can significantly increase. But one of the options for solving this problem is the implementation of this concept of building an image processor on analog devices, for example, on current mirrors, i.e. the use of processing in analog or hybrid formats. Similar conceptual approaches were proposed in the works [21, 22], where the developed and modeled so-called equivalent neurons were described, which have a processing-conversion time of 0.1-1μs, low supply voltages of 1.8-3.3V, insignificant relative computational errors (1-5%), low consumption of no more than 1-2mW, can operate in low power consumption modes (less than 100μW) and high-speed (10-20MHz) modes. Therefore, it is necessary to further conduct a comparative analysis of these two (digital and analog) formats for implementing the proposed concept of building multifunctional image processors. Their comparison is especially important from the point of view of efficiency relative to energy consumption, since the efficiency of neuro-equivalentors relative to energy

consumption is estimated at a level of no less than 10^{12} an. op./s per W and can be increased by an order of magnitude [21, 22].

The developed processors can become the basis for the implementation of convolutional NNs and self-learning biologically inspired devices with a code-controlled choice of the type of nonlinear, as well as linear, functional transformation and a significant number of processing channels due to the integration of an array of neural-like processors into a chip to implement parallel computing of equivalental convolutions.

IV. CONCLUSIONS

We show the results of design the new FPGA-DMIPs with digital accuracy. Calculations show that in the case of using Altera FPGA chip EP3C16F484 of Cyclone III family, it is possible to implement DMIP for image size of 64×64 and window 3×3 in the one chip. For 2.5V and clock frequency of 200MHz the power consumption will be at the level of 200mW and the calculation time for pixel of filters will be 25ns.

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